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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	FINN et al.
Serial No	:	
Confirm. No.	:	
Filed	:	
For	:	CHIP CARRIER FOR...
Art Unit	:	
Examiner	:	
Dated	:	November 2, 2001

Hon. Commissioner of Patents
and Trademarks
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Attached please find Form PTO-1449 together with the references for the above identified application that include, with others, references as stated in corresponding examination procedures and International Search Report.

DE 195 41 039 has been cited in corresponding foreign examination procedures. This reference discloses a chip module for a chip card having chip and a substrate in contact with it and an insulating layer on the substrate. The terminal conductors stretch, side by side with a gap, on the insulation layers. The chip is made with two spigots that pass through a passivation layer and project beyond this. These spigots are the contact metallisations engaging in the terminal conductors and locate these in position. In addition, to provide good electrical contact between the terminal conductors and the contact region

for the chip, the recesses are filled with bonding material which conducts well. No translation of this reference is available to Applicant at this time.

US 5,681,662 has been cited in foreign corresponding examination procedures and discloses copper alloy foils for flexible circuits.

US 5,847,929 has been cited in foreign corresponding examination procedures and discloses attaching heat sinks directly to flip chips and ceramic chip carriers.

US 5,426,399 has been cited in foreign corresponding examination procedures and discloses film carrier signal transmission line having separating grooves.

EP 0 391 790, which corresponds to US 5,041,391, has been cited in foreign corresponding examination procedures discloses a method of encapsulation an integrated circuit using a punched metal grid attached to a perforated dielectric strip having the encapsulation of integrated circuit chips, notably with a view to their being incorporated in a chip card. The encapsulation method comprises the formation of a pre-punched metallic conductive grid, the formation of a strip of pre-perforated plastic material, the transfer of a strip to the grid, the positioning of an integrated circuit chip in a perforation of the strip, and the formation of electrical connections between the chip and zones of the grid located in perforations of the strip. The perforations of the strip and the punched slots of the grid are arranged so that the strip covers and blocks all the interstices between conductors of the grid in the useful region corresponding to a module to be made. When a protecting resin is laid, it is confined and does not leak through the interstices of the grid. A plastic or metal ring defines the heightwise dimension of the micromodule. No translation of this reference

is available to Applicant at this time.

FR 2 756 955 has been cited in foreign corresponding examination procedures discloses a method for producing an electronic circuit for an electronic chip card for non-contact data exchange having a reading device, said electronic circuit comprising an antenna for being coupled with said reading device and a semiconductor chip connected to said antenna. The invention is characterized in that it consists of the following steps: a) producing on a plastic support-sheet a coupling antenna provided with two terminals for electrical connection; b) mounting on said terminals for electrical connection a semiconductor chip with contact by protrusions. The invention is applicable for making contactless cards. No translation of this reference is available to Applicant at this time.

DE 196 01 203 as cited in the International Search Report under category Y for claims 1-4, 6, 8 and 10-14. This reference discloses a data carrier card incorporating semiconductor chip having a flat plastic body with a flat recess in one surface for receiving the semiconductor chip, containing 3-dimensional conductor paths for directly contacting the inserted chip. The conductor paths may act as a bus system for contacting a number of inserted chips, each of which is enclosed by a protective plastics cover layer, preventing mechanical damage and corrosion. No translation of this reference is available to Applicant at this time.

EP 0 421 343 as cited in the International Search Report under category Y for claims 1-4, 6, 8 and 10-14. This reference discloses a semiconductor element package and a semiconductor element package mounting distributing circuit basic plate, wherein the shield

metallic layer is provided on the flexible insulating basic plate for constituting the package, so that the semiconductor element mounted on the flexible insulating basic plate may be kept electromagnetically shielded positively with the shield metallic layer, whereby troublesome operation such as mounting the bulk high box shaped electromagnetic shield member on the outside of the semiconductor element package mounted on the distributing circuit basic plate as in the conventional one is not required, and, also, since the shield metallic layer is provided on the face, which is not formed with the lead patterns, of the flexible insulating basic plate, no influences are applied at all upon the construction of the land pattern and the mounting construction of the semiconductor element.

EP 0 682 321 as cited in the International Search Report under category A for claims 5, 7 and 9. This reference discloses a record carrier with integrated circuit having a chip card with a rectangular card body, with one or more layers, incorporating an IC chip and at least one coil, for energy supply and/or data exchange between the IC and an external card reader. The IC and at least 2 contact elements are incorporated in a module positioned so that the contact elements are electrically connected to the coil terminals. Pref. the coil is provided as a flat coil applied to an insulating layer of the card body as a stamped out metal foil, or a screen printed metal layer. No translation of this reference is available to Applicant at this time.

DE 196 39 646 as cited in the International Search Report under category A for claims 5, 7 and 9. This reference discloses carrier element for semiconductor chip with the carrier element having an electrically conductive foil laminated with an electrically insulating

foil. The electrically conductive foil is structured to provide contact surfaces for electrically contacting the semiconductor chip, both foils coupled together via an adhesive-free connection. Preferably the side of the electrically conductive foil facing the electrically insulating foil is structured to provide projections which penetrate the surface of the electrically insulating foil when he foils are pressed together. No translation of this reference is available to Applicant at this time.

US 5,744,859 as cited in the International Search Report under category A for claims 1 and 8. This reference discloses semiconductor device.

For the convenience of the Examiner Applicant attaches a copy of the International Search Report.

Consideration of the various references is requested.

Respectfully submitted
for Applicant,

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JJM:/kdm/esd

Enclosed: PTO-1449 Form
11 References
International Search report

DATED: November 2, 2001
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SHOULD ANY OTHER FEE BE REQUIRED, THE PATENT AND TRADEMARK OFFICE IS HEREBY REQUESTED TO CHARGE SUCH FEE TO OUR DEPOSIT ACCOUNT 13-0410.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231,NO.: EL 346 229 420 US

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BY: _____ DATE: November 2, 2001

Form PTO-1449 U.S. Department of Commerce Patent and Trademark Office Sheet 1 of 1

LIST OF REFERENCES CITED BY APPLICANT
(Use several sheets if necessary)

Atty Docket No.: 70357
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Group:

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date
	US 5,681,662	Oct. 28, 1997	Chen et al.			Sep. 15, 1995
	US 5,847,929	Dec. 8, 1998	Bernier et al.			Jun. 28, 1996
	US 5,426,399	Jun. 20, 1995	Matsubayashi et al.			Dec. 13, 1993
	US 5,744,859	Apr. 28, 1998	Ouchida			Feb. 7, 1996

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Country	Class	Sub-class	Translation Yes/No
	DE 195 41 039 A1	May 7, 1997	Germany			No
	DE 196 01 203 A1	Mar. 20, 1997	Germany			No
	EP 0 421 343 A2	Apr. 10, 1991	European			Yes
	EP 0 682 321 A2	Nov. 15, 1995	European			No

	DE 196 39 646 A1	Mar. 2, 1998	Germany			No
	EP 0 391790 A1	Oct. 10, 1990	European			No
	FR 2 756 955 A1	Jun. 12, 1998	French			No

Examiner

Date Considered